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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,017	01/22/2002	Bruce James Wilkie	RPS920010090US1	8725

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EXAMINER	
BADERMAN, SCOTT T	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,017	WILKIE, BRUCE JAMES	
	Examiner	Art Unit	
	Scott T Baderman	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: In line 3, "the processors" lacks antecedent basis. Appropriate correction is required.

2. Claim 20 is objected to because of the following informalities: In line 2, "the error status signals" lacks antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-6, 10-11, 13-15, 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Bouvier et al. (5,530,946).

As in claims 1 and 10, Bouvier discloses a data processing system, comprising: at least one main processor connected to a system bus (Figure 1); a system memory connected to the system bus and accessible to each of the processors (Figure 1); error logic (Figure 2, element 240) configured to receive internal error signals (Figure 3, element 318) asserted by one or more

of the main processors and to respond to an internal error signal by disabling the processor asserting the signal and restarting the system with any remaining functional processors (Figures 2-4, Abstract, column 3: lines 10-31, column 6: lines 35-43).

As in claims 2 and 11, Bouvier discloses a system wherein the error logic is further configured to record the internal error signal in an error status register of the error logic (Figure 2, column 3: lines 18-31, column 6: lines 44-62).

As in claims 4 and 13, Bouvier discloses a system wherein the error logic is functional substantially immediately following the application of power to the data processing system (Figure 3, column 5: line 55 – column 6: line 22).

As in claims 5 and 14, Bouvier discloses a system wherein the error logic includes an error detection unit configured to receive an internal error signal from each of the main processors and further configured to generate an error detect signal responsive to assertion of an internal error signal by any of the processors (Figure 2, Abstract, column 6: lines 35-43. column 8: lines 39-50).

As in claims 6 and 15, Bouvier discloses a system wherein the error logic further includes error logging logic configured to receive the error detect signal and, responsive thereto, to update an error status register to reflect the internal error signal (Figure 2, column 6: lines 35-62).

As in claim 17, the Applicant is directed to claims 1, 5 and 6 above.

As in claim 18, Bouvier discloses a method wherein updating the error status register includes updating a current status bit for each of the main processors based on the current state of the corresponding internal error signal (column 7: lines 50-53, column 8: lines 18-50).

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Bossen et al. (6,233,680).

As in claims 1 and 10, Bossen discloses a data processing system, comprising: at least one main processor connected to a system bus; a system memory connected to the system bus and accessible to each of the processors; error logic configured to receive internal error signals asserted by one or more of the main processors and to respond to an internal error signal by disabling the processor asserting the signal and restarting the system with any remaining functional processors (column 1: line 5 – column 4: line 30).

As in claims 2 and 11, Bossen discloses a system wherein the error logic is further configured to record the internal error signal in an error status register of the error logic (column 1: line 5 – column 4: line 30).

As in claims 3 and 12, Bossen discloses a system wherein the error status register includes at least a pair of bits corresponding to each of the main processors, wherein a first bit of each pair is indicative of whether the corresponding main processor is currently asserting its internal error signal and a second bit of each pair is indicative of whether the corresponding main processor has asserted its internal error signal previously (column 1: line 5 – column 4: line 30).

As in claims 4 and 13, Bossen discloses a system wherein the error logic is functional substantially immediately following the application of power to the data processing system (column 1: line 5 – column 4: line 30).

As in claims 5 and 14, Bossen discloses a system wherein the error logic includes an error detection unit configured to receive an internal error signal from each of the main processors and further configured to generate an error detect signal responsive to assertion of an internal error signal by any of the processors (column 1: line 5 – column 4: line 30).

As in claims 6 and 15, Bossen discloses a system wherein the error logic further includes error logging logic configured to receive the error detect signal and, responsive thereto, to update an error status register to reflect the internal error signal (column 1: line 5 – column 4: line 30).

As in claims 7 and 16, Bossen discloses a system wherein the error logic is further configured to generate a service processor interrupt responsive to error status register update (column 1: line 5 – column 4: line 30).

As in claim 8, Bossen discloses a system wherein the data processing system further includes a service processor configured to receive the service processor interrupt from the error logic (column 1: line 5 – column 4: line 30).

As in claim 9, Bossen discloses a system wherein responsive to the service processor interrupt, the service processor is configured to powering down the system (column 1: line 5 – column 4: line 30).

As in claim 17, the Applicant is directed to claims 1, 5 and 6 above.

As in claims 18 and 20, the Applicant is directed to claim 7 above.

As in claim 19, the Applicant is directed to claim 3 above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7-9, 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bouvier et al..

As in claims 7, 16 and 20, Bouvier discloses a system wherein the error logic is further configured to signal a service processor (control unit) responsive to error status register update (i.e., when the error bit is set) (column 7: lines 32-39, column 8: lines 18-50). However, Bouvier does not specifically disclose generating an interrupt.

It would have been obvious to a person skilled in the art at the time the invention was made to include generating an interrupt into the system taught by Bouvier above. This would have been obvious because the definition of an interrupt is "a request for attention from a processor". Based on this definition, a person skilled in the art would have understood that by

setting the error bit (column 8: lines 22-24) which causes the control unit to perform a reset would be getting the attention of the control unit, and hence, be interpreted as an interrupt.

As in claim 8, Bouvier discloses a system wherein the data processing system further includes a service processor (control unit) configured to receive the service processor interrupt from the error logic (column 7: lines 32-39, column 8: lines 18-50).

As in claim 9, Bouvier discloses a system wherein responsive to the service processor interrupt, the service processor is configured to powering down (reset) the system (Figure 2, column 8: lines 18-50).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T Baderman whose telephone number is (703) 305-4644. The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Scott T Baderman
Primary Examiner
Art Unit 2113

STB